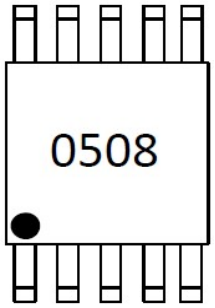
8-Line Ultra Low Capacitance TVS Diode Array

Features

- Very low capacitance : 0.6pF typical
- Low operating voltage : 5V
- Low clamping voltage
- Protects one power line and 8 data lines
- Flow-through package
- Complies with following standards :
  - IEC 61000-4-2(ESD) immunity test
    Air discharge : ±25kV, Contact discharge : ±20kV
  - IEC61000-4-5 (Lightning) 5A (8/20us)
- RoHS Compliant

Marking Inforamtion

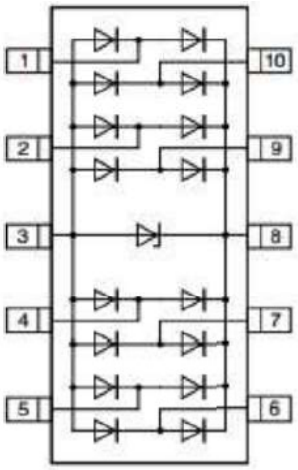


0508 = Device Marking Code
YYWW= Date Code
Dot denotes pin1

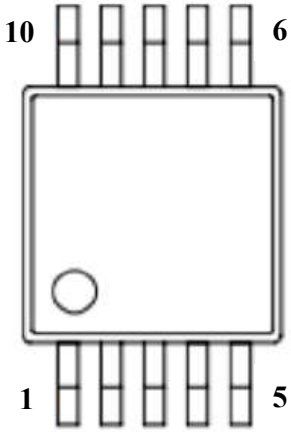
Mechanical Data

- Package : MSOP-10
- Case Material : "Green" Molding Compound.
- Lead Finish : Matte Tin
- UL Flammability Classification Rating 94V-0
- Moisture Sensitivity : Level 3 per J-STD-020
- Terminal Connections : See Diagram Below
- Marking Information : See Below

Circuit and Pin Schematic



Circuit Diagram



Pin Schematic

Applications

- DVI Ports
- HDMI Ports
- USB 2.0
- High-Speed Data Lines

Absolute Maximum Ratings (Ta= 25℃ unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20us)	Ppk	80	W
Peak Pulse Current (8/20us)	Ipp	5	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±25 ±20	kV
Operating Junction Temperature Range	T_J	-55 to +125	℃
Storage Temperature Range	T_{STG}	-55 to +150	℃

Electrical Charateristics (Ta= 25℃ unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Reverse Working Voltage	V_{RWM}	-	-	5.0	V	Pin 3 to 8
Breakdown Voltage	V_{BR}	6.0	-	-	V	I_T = 1mA, Pin 3 to 8
Reverse Leakage Current	I_R	-	-	0.2	uA	V_{RWM} =5V, Pin 3 to 8
Clamping Voltage (any I/O pin to ground)	V_C	-	-	10	V	I_{PP}=1A(8×20us pulse)
Clamping Voltage (any I/O pin to ground)	V_C	-	-	16	V	I_{PP}=5A(8×20us pulse)
Junction Capacitance (between I/O pins)	C_J	-	0.3	0.5	pF	f=1MHz, V_R=0V
Junction Capacitance (any I/O pin to ground)	C_J	-	0.6	-	pF	f=1MHz, V_R=0V

Ratings and Characteristics Curves (Ta=25℃ unless otherwise noted)

Fig.1 Power Derating Curve

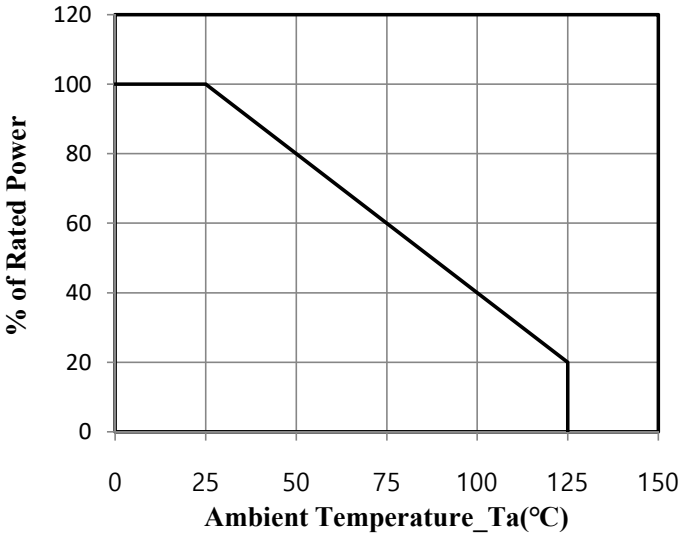


Fig.2 Peak Pulse Power vs. Pulse Time

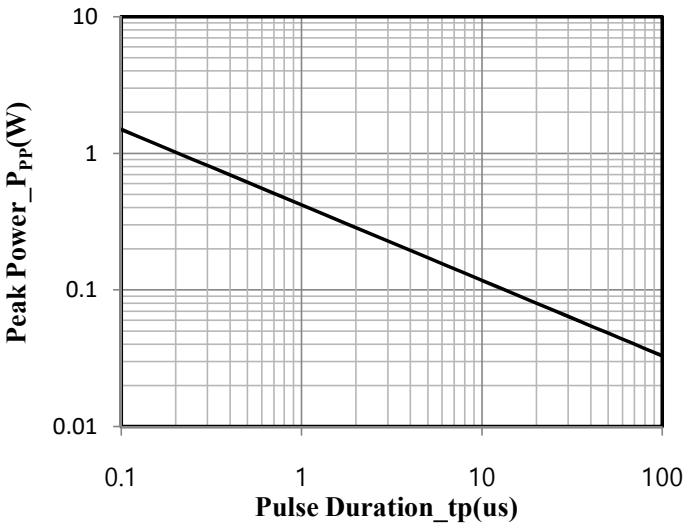


Fig.3 Clamping Voltage vs. Peak Pulse Current (tp=8/20us)

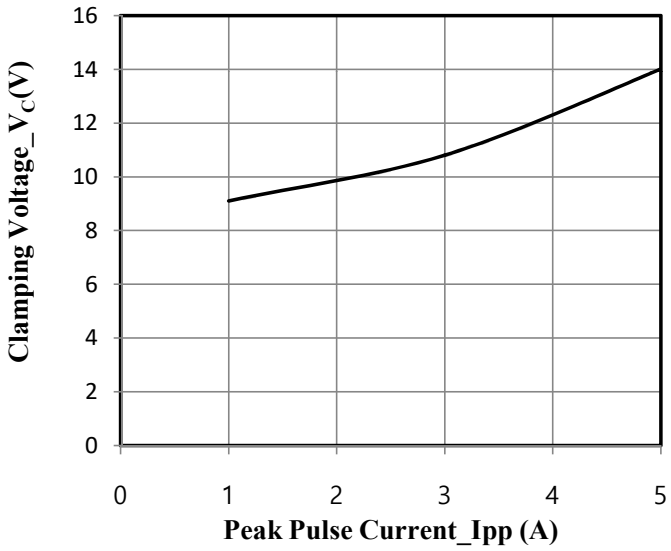


Fig.4 Junction Capacitance vs. Reverse Voltage

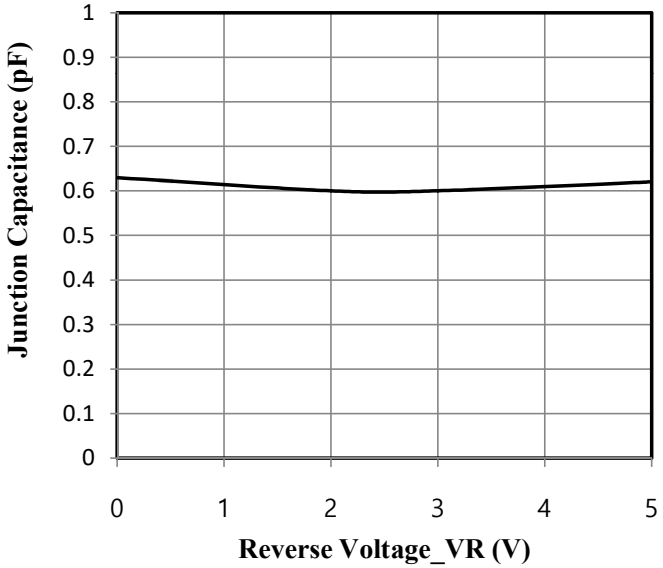


Fig.5 8 × 20us Pulse Waveform

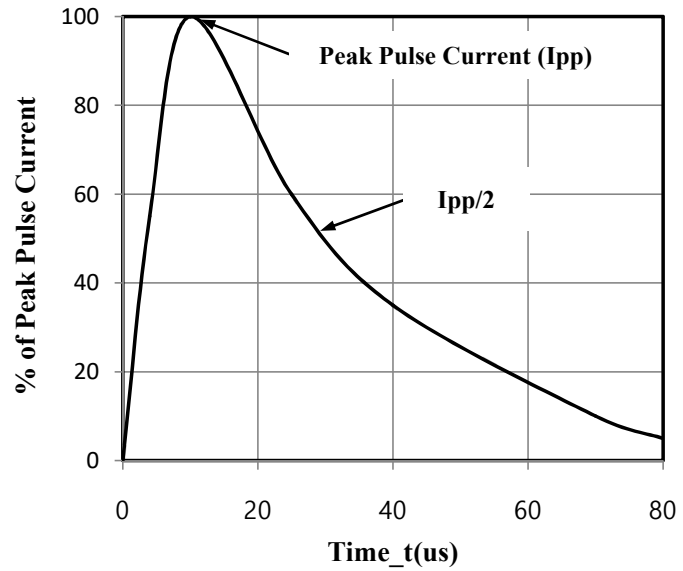
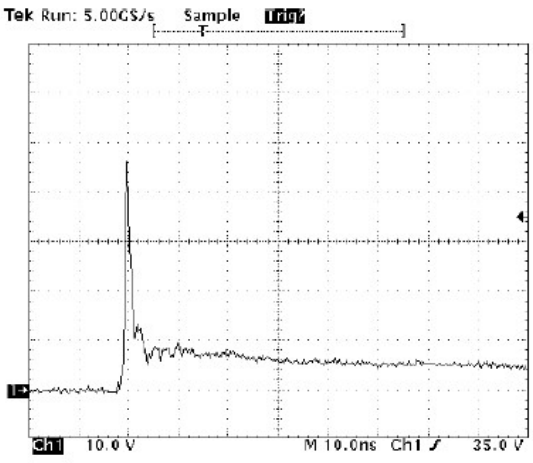
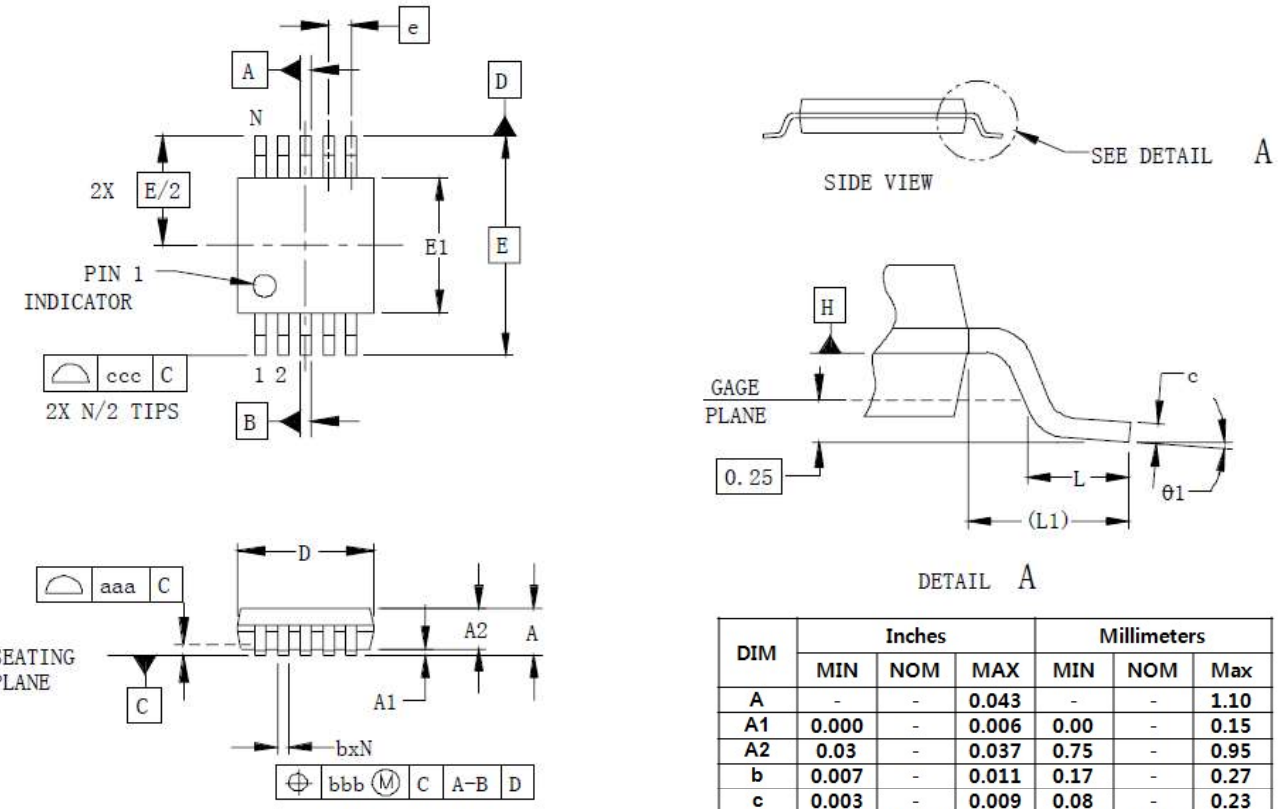


Fig. 6 ESD Clamping Voltage 8kV Contact per IEC61000-4-2



Note：Data is taken with a 10x attenuator

MSOP-10 Package Outline Drawing

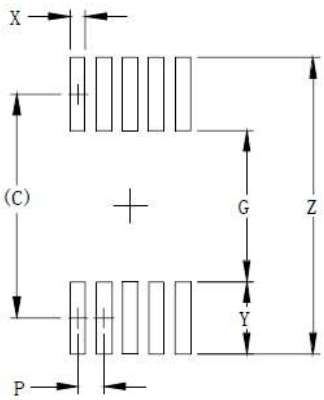


DIM	Inches			Millimeters		
	MIN	NOM	MAX	MIN	NOM	Max
A	-	-	0.043	-	-	1.10
A1	0.000	-	0.006	0.00	-	0.15
A2	0.03	-	0.037	0.75	-	0.95
b	0.007	-	0.011	0.17	-	0.27
c	0.003	-	0.009	0.08	-	0.23
D	0.114	0.118	0.122	2.90	3.00	3.10
E1	0.114	0.118	0.122	2.90	3.00	3.10
E	0.193 BSC			4.90 BSC		
e	0.020 BSC			0.50 BSC		
L	0.016	0.024	0.032	0.40	0.60	0.80
L1	(0.037)			(0.95)		
N	10			10		
θ1	0°	-	8°	0°	-	8°
aaa	0.004			0.10		
bbb	0.003			0.08		
ccc	0.010			0.25		

Notes :

1. Controlling dimensions are in millimeters (Angles in Degress).
2. Datums A and B to be determined at datum plane H
3. Dimensions " E1" and "D" do not include mold flash, protrusions or gate burrs.
4. Reference JEDEC STD MO-187, Variation BA.

Suggested Land Pattern



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.020	0.50
X	.011	0.30
Y	.063	1.60
Z	.224	5.70

Notes :

1. This land pattern is for reference purposes only.
   Consult your manufacturing group to ensure your company's manufacturing guidelines are met.